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For: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME	

Commissioner for Patents
Alexandria, VA 22314

Sir:

VERIFICATION OF A TRANSLATION FOR JP APPLICATION 2001-6581

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The document for which the attached English translation is being submitted is Japanese Patent Application No. 2001-6581 filed in Japan on January 15, 2001. The Japanese language document was submitted to the U.S. Patent and Trademark Office on January 14, 2002 as the certified copy of the foreign priority application.

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[FILED DOCUMENT NAME] Abstract 1

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[Title of the Invention] SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

[Scope of the Claims]

[Claim 1] A semiconductor device comprising:

an interconnection layer arranged above a surface of a substrate on which a functional semiconductor region is formed;

an inter layer dielectric covering a surface of said interconnection layer, and

a silicon nitride film formed so as to cover a whole surface of said inter layer dielectric;

a metal interconnection layer as an uppermost metal layer formed as an upper layer of said silicon nitride film, said metal interconnection layer being consisted of gold material; and

a planarized dielectric formed on said metal interconnection layer.

[Claim 2] A semiconductor device according to claim 1, wherein said planarized dielectric is consisted of polyimide.

[Claim 3] A semiconductor device according to claim 2, wherein said silicon nitride film is formed by high-density plasma CVD method.

[Claim 4] A semiconductor device according to claim 1, wherein polyimide resin layer is removed at a part of region of said metal interconnection layer and bonding wire is connected to said region in said metal interconnection layer.

[Claim 5] A method for manufacturing a semiconductor device

comprising steps of:

a process for forming a foundation interconnection layer on a surface of a semiconductor substrate on which a functional semiconductor region is formed;

a process for forming an inter layer dielectric on said foundation interconnection layer of which surface is shaped as convex and concave shape;

a process for forming silicon nitride film on said inter layer dielectric;

a process for forming metal interconnection layer as an uppermost layer interconnectionas an upper layer of said silicon nitride film, said metal interconnection layer being consisted of gold; and

a process for coating a polyimide resin film on said metal interconnection layer and planarizing surface thereof.

[Claim 6] A method for manufacturing a semiconductor device according to claim 5, wherein said metal interconnection layer is connected to said foundation interconnection layer through a though hole formed in-between thereof and furhter wherein said interconnection layer is low in resistance and formed thicker than thickness of said foundation interconnection layer.

[Claim 7] A method for manufacturing a semiconductor device according to claim 6, wherein said method further includes a process for removing a part of region of said polyimide resin layer, and a process for wire-bonding at said part of region so as to connect to a surface of said metal interconnection layer.

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention Belongs]

The present invention relates to a semiconductor device and a method for manufacturing the semiconductor device, particularly to the uppermost layer interconnection and passivation structure thereof.

[0002]

[Conventional Arts]

Various kinds of techniques are known for planarizing an upper surface of the inter-metal dielectric, at manufacturing a semiconductor device of VLSI (Very Large Scale Integrated Circuit) and the like. The semiconductor device manufactured using the conventional technique of planarizing the inter-metal dielectric is shown in Fig. 1.

[0003]

According to the conventional method for manufacturing, first, an object forming field oxide film 2 on a semiconductor substrate 1 is prepared and a MOSFET (Metal-Oxide-Silicon Field Effect Transistor) having a poly silicon gate 5 is formed on the field oxide film 2 and semiconductor substrate 1 as shown in Fig. 6.

[0004]

Next, ILD (Inter Layer Dielectric) 3 is formed so as covering them. The inter layer dielectric 3 consists of PSG (Silicon oxide doping Phosphorus) or BPSG (Silicon oxide doping Boron and

Phosphorus). Next, aluminum interconnection 4 is formed on the inter layer dielectric 3.

[0005]

By depositing USG (Silicon glass not doped) using CVD method (Vapor phase epitaxy method) and the like, USG layer 6 is formed.

[0006]Next, after forming aluminum interconnection 7s as the uppermost layer metal interconnection, and forming passivation film and PSG (Silicon oxide doping Phosphorus) or BPSG (Silicon oxide doping Boron and Phosphorus) 8, SOG film 8s is formed so as to planarized surface.

[0007]Thus, although planarization of the surface is carried out with forming the passivation film, there are problems that passivation film of enough film thickness must be formed to protect completely aluminum interconnection of foundations and that it takes time for forming film.

[0008]

Moreover, bonding is need for the uppermost layer interconnection and it needs to form an electrode pat superior in bonding resist. Therefore, it is need that only a part of the bonding pad is formed separately or that thickness of film is made thick enough at the case forming it on the same process. Therefore, roughness of the surface is made large, so there is a problem that planarizing process of the passivation film forming on the upper layer is difficult.

[0009]Further more, in the SOG process, many process and operations are need. For example, before removing unnecessary

part by etching-back after applying SOG layer, measuring process of thickness of film of the applied SOG layer and annealing process of the applied SOG layer, and in the etching-back process of the SOG layer, operation of measuring thickness of the remained film is need. Moreover, after the etching-back process, O_2 plasma processing process, scrubber process using a brush, and so on are need. Further more, although silicon compound (generally $R_nSi(OH)_{4-n}$) is used for insulation material, there is a problem that it is comparatively expensive.

[0010]

[Problems that the Invention is to Solve]

As described above, in the conventional interconnection structure, there are problems such that manufacturability is low or it is difficult to keep reliability.

[0011]

An object of the invention is to provide a method for manufacturing a semiconductor device forming a interconnection structure installing a passivation structure having a flat upper surface which is easy to manufacture and is superior in insulation performance with low cost and short lead time in order to solve these problems.

Moreover, an another object is to provide a interconnection structure in which interconnection resistance is small and bonding resist is high.

[0012]

[Means for Solving the Problems]

Then, the first invention is characterized in including interconnection layer formed on surface of a substrate forming desired element region, inter layer dielectric covering surface of said interconnection layer, silicon nitride film formed so as covering whole surface of said inter layer dielectric, metal interconnection layer consisting of gold layer as the uppermost lay metal formed on the upper layer of said silicon nitride film, and planarized dielectric formed on said metal interconnection layer.

[0013]

According to its structure, as the metal interconnection layer of the uppermost layer is structured with gold, the interconnection layer can be made low resistance and thin in film thickness thereof so that planarizing surface is easy.

[0014]

As the metal interconnection layer of the uppermost layer is structured with gold, humidity resistance can be made high and it is possible to simplify passivation structure comparing with that of the conventional interconnection such as aluminum interconnection. Surface of the inter layer dielectric of foundation is protected by silicon nitride film. In the region where a through hole is formed on the silicon nitride film, its surface is covered with metal layer as the uppermost layer metal interconnection layer, therefore, protection of the lower layer interconnection region and the semiconductor element region is perfect.

[0015]

As the inter layer dielectric such as USG film is covered with silicon nitride film, it is fine to film thickness and passivation effect is high. Therefore, the passivation film formed on the upper layer may be an object low in passivation effect. Therefore, the passivation film is only polyimide film and it is possible to obtain planarized structure easily and in short time.

[0016] Further, the invention is characterized by said planarized dielectric made of polyimide.

It is possible to form thick film in film thickness extremely easily by applying process because polyimide is used for the planarized film.

[0017] As the metal interconnection of the uppermost layer is structured with gold layer, enough passivation effect can be obtained even if polyimide is formed directly. Further, it is possible to use the metal interconnection directly as a bonding pad.

[0018] Further, the invention is characterized by said silicon nitride film being formed by high-density plasma CVD method.

[0019]

According to the method, fine film can be formed by forming the inter layer dielectric by vapor phase epitaxial method using high-density plasma superior in embedding facility. Moreover, inter layer dielectric which is planarized at the upper face can be formed efficiently.

[0020]

Further, the invention is characterized by polyimide resin layer being removed at a part of region of said metal interconnection layer and bonding wire is connected to said region in said metal interconnection layer.

[0021]

According to the structure, by removing polyimide only at necessary region of periphery and carrying out bonding, it is possible to decrease sharply probability of occurrence of shortage and to design improvement of yield.

[0022]

At direct bonding, forming a bump is very easy by forming a through hole at polyimide film using photolithography method and carrying out gold selective plating.

[0023]

As high SOG process in production cost can be omitted, production cost can be decreased. Lead time for production can be shortened. Therefore, cost required for forming the inter-metal dielectric can be decreased and shortening of production lead time can be designed.

[0024]

That is, it is possible to form inter layer dielectric having flat upper face superior in insulation performance with low cost and short lead time.

[0025]

[Mode for Carrying out the Invention]

Fig. 1 is a main part view showing a semiconductor device according to a mode for carrying out the invention. Figs. 2 to 5 show a part of sectional structure of semiconductor at each manufacturing process.

[0026]

The semiconductor device forms a MOSFET (Metal Oxide Silicon Field Effect Transistor) having a poly silicon gate 5 on a silicon substrate 1 forming field oxide film as shown in Fig. 1.

[0027]

That is, the semiconductor is characterized in including a first interconnection layer 14 consisting of aluminum formed on surface of a silicon substrate 11 forming desired element region, inter layer dielectric 16 consisting of USG film covering surface of said first interconnection layer 14, silicon nitride film 16s formed by plasma CVD method as covering whole surface of said inter layer dielectric 16, metal interconnection layer 19 consisting of gold layer as the uppermost lay metal formed on the upper layer of said silicon nitride film 16s, and planarized dielectric 18 consisting of polyimide film formed on said metal interconnection layer 19. Between the metal interconnection layer 19 and the first interconnection layer 14, barrier layer 19s consisting of thin titanium film in order to prevent migration of aluminum is stood.

[0028]

Field oxide film 12 is formed on the silicon substrate 11, the MOSFET having the poly silicon gate 15 is formed, and inter

layer dielectric 13 is formed as covering this. The inter layer dielectric 13 consists of PSG (silicon oxide film doping phosphorus) or BPSG (silicon oxide film doping boron and phosphorus) for example.

[0029]

Next, the manufacturing process of the semiconductor device will be described.

First, with forming an element region by forming element separation film 12 on surface of a silicon substrate 11, a MOSFET having gate interconnection 15 consisting of poly silicon film in the element region as shown in Fig. 2.

[0030]

Inter layer dielectric 13 consisting of BPSG film is formed on the upper layer and a first interconnection layer 14 connecting to the gate interconnection through a contacting hole not shown is formed as shown in Fig. 3.

[0031]

After that, USG layer 16 is formed by depositing USG (silicon glass not doped) by CVD method (Vapor phase epitaxy method) and the like, further silicon nitride film 16s is formed on the upper layer by plasma CVD method as shown in Fig. 4.

A contacting hole H for forming metal interconnection of the uppermost layer is formed.

[0032]

After that, metal interconnection 19 consisting of gold layer is formed after forming titanium thin film for barrier

layer 19s by spattering method as shown in Fig. 5.

[0033]

After that, passivation film 18 consisting of polyimide film of two microns film thickness is formed by applying method.

[0034]

Thus, the semiconductor device shown in Fig. 1 is formed.

[0035]

According such the structure, bonding facility is superior, resistance is low, and reliability is high as the metal interconnection layer of the uppermost layer is structured with gold layer. Further, as thickness of film of the interconnection layer can be made thin, it is easy to planarize the surface.

[0036]

AS the metal interconnection layer of the uppermost layer is structured by gold, humidity resistance can be made high and it is possible to simplify passivation structure comparing with the conventional interconnection such as aluminum interconnection. Surface of the inter layer dielectric of foundation is protected by silicon nitride film formed using plasma CVD method and it is fine so as to be superior in passivation effect even it is thin.

[0037]

As film thickness is thin, roughness of the upper layer is small so that planarizing process is easy.

[0038]

In the region where the through hole is formed on the silicon

nitride film, surface thereof is covered with metal layer as the uppermost layer metal interconnection layer, therefore, protection effect of the lower layer interconnection region and the semiconductor element region is high and reliability is high.

[0039]

As the inter layer dielectric such as USG film is covered with silicon nitride film, it is fine in film thickness and passivation effect is high. The passivation film formed on the upper layer may be an object low in passivation effect. Therefore, the passivation film is only polyimide film and it is possible to obtain planarized structure easily and in short time.

[0040]

It is possible to form thick film in film thickness extremely easily by applying process because polyimide is used for the planarized film.

[0041]

As the metal interconnection of the uppermost layer is structured with gold layer, enough passivation effect can be obtained even if polyimide is formed directly. Further, it is possible to use the metal interconnection directly as a bonding pad.

[0042]

Fine film can be formed by forming the inter layer dielectric with vapor phase epitaxy method using high-density plasma superior in embedding facility. Inter layer dielectric flat at the upper face can be formed efficiently.

[0043]

By removing polyimide only at necessary region of periphery and carrying out bonding, it is possible to decrease sharply probability of occurrence of shortage and to design improvement of yield.

[0044]

At direct bonding, forming a bump is very easy by forming a through hole at polyimide film using photolithography method and carrying out gold selective plating. As periphery of the bump is polyimide film, it is elastic and bonding is easy.

[0045]

As high SOG process in production cost can be omitted, production cost can be decreased. Lead time for production can be shortened so that cost required for forming inter-metal dielectric can be decreased. Further, shortening of production lead time can be designed.

[0046]

That is, it is possible to form inter layer dielectric having flat upper face superior in insulation performance with low cost and short lead time.

[0047]

For the inter layer dielectric, PSG (silicon oxide film doping phosphorus) and USG film are applicable except BPSG.

[0048]

Silicon nitride may be formed by high density plasma CVD method after applying organic SOG layer structured with organic

dielectric (organic SOG) consisting of silicon compound easily forming thickness on the deposited USG layer using SOG (Spin On Glass) method and embedding concave portion of the upper face of the USG layer.

[0049]

As the high density plasma CVD method is good in embedding performance, it is possible that the upper face of the USG layer is kept flat and that the concave portion is embedded.

[0050]

After that, inter-metal dielectric having a structure surrounding SOG layer with good USG layer in film quality and being high insulation performance is formed after washing process, SOG annealing process, and so on.

[0051]

The high density plasma CVD method can carry out forming film by CVD method and etching by spattering at the same time so as to carry out film forming superior in embedding performance. For plasma source of the high-density plasma CVD apparatus, an object using ECR (electron cyclotron resonance), ICP (inductively coupled plasma), and so on are known.

[0052]

The high-density plasma CVD apparatus uses the ICP (inductively coupled plasma) for the plasma source. The high-density plasma CVD apparatus has a ceramic dome of hemisphere shape, and at outer circumference of the ceramic dome, coil structured with copper is arranged. The coil is applied with

low frequency power of about 300 kHz to 2 MHz. High density plasma (10^{11} to 10^{12} [ions/cm^3]) is formed by inductively coupled energy based on the low frequency power.

[0053]

The SOG process high in production cost can be replaced with applying process of polyimide film. Because of that, production cost can be decreased according to needlessness of process forming the SOG process and lead-time required for production can be shortened. Therefore, it is possible to decrease cost required for forming inter layer dielectric and to shorten production lead-time.

[0054]

That is, it is possible to form inter layer dielectric having a flat upper face superior in insulation performance with low cost and short lead-time.

[0055]

Although interconnection layer of the MOSFET structured with the field oxide film and the aluminum interconnection formed thereon as foundation layer is described for example in the above-mentioned mode for carrying out, foundation layer is not limited to this. The foundation layer in the invention means whole conductive layer having surface of convex and concave shape.

[0056]

[Advantages of the Invention]

According to the invention, by using gold for the uppermost layer metal interconnection and forming silicon nitride film on inter

layer dielectric, passivation effect is made high, therefore, it is possible to provide a semiconductor device easy in manufacturing and high in reliability.

[Brief Description of the Drawings]

[Fig. 1]

Fig. 1 is a view showing a semiconductor device according to a mode for carrying out the invention.

[Fig. 2]

Fig. 2 is a view showing a method for manufacturing a semiconductor device according to the mode for carrying out the invention.

[Fig. 3]

Fig. 3 is a view showing a method for manufacturing a semiconductor device according to the mode for carrying out the invention.

[Fig. 4]

Fig. 4 is a view showing a method for manufacturing a semiconductor device according to the mode for carrying out the invention.

[Fig. 5]

Fig. 5 is a view showing a method for manufacturing a semiconductor device according to the mode for carrying out the invention.

[Fig. 6]

Fig. 6 is a view showing the conventional semiconductor device.

[Description of the Reference Numerals and Signs]

12 FIELD OXIDE FILM

14 ALUMINUM INTECONNECTION

16 USG LAYER

16s PLASMA SILICON NITRIDE LAYER

18 POLYIMIDE FILM

19 GOLD LAYER

19s Ti LAYER

[Identification of Document] Abstract

[Abstract]

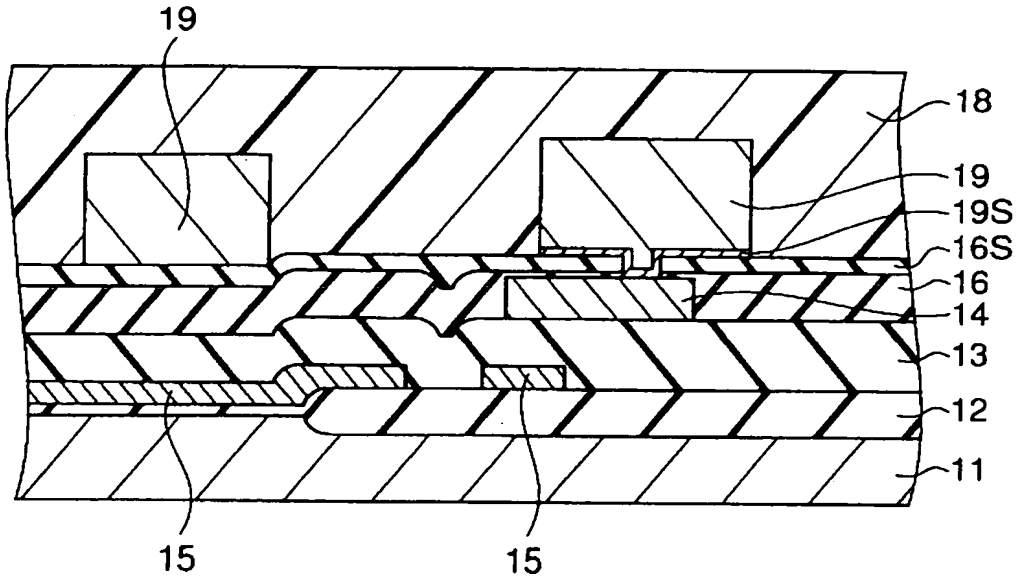
[Problem] To form a interconnection structure easy in manufacturing, superior in insulation performance, and providing a passivation structure having a planarized upper face (surface) with low cost and short lead-time.

[Means for Solution] The invention is characterized in including wiring layer formed on surface of a substrate forming desired element domain, inter metal dielectric covering surface of said wiring layer, silicon nitride film formed so as covering whole surface of said inter layer dielectric, metal wiring layer consisting of gold layer as the highest lay metal formed on the upper layer of said silicon nitride film, and planarized dielectric formed on said metal wiring layer.

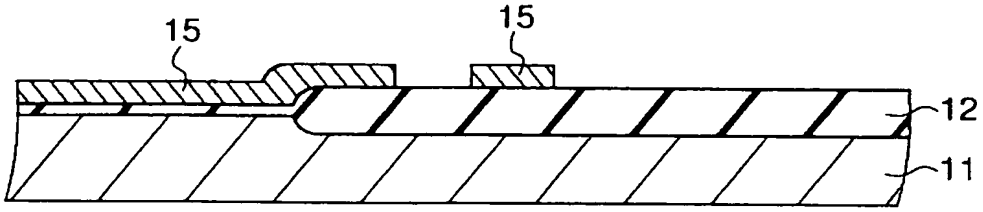
[Selected Drawing] Fig. 1

【書類名】　図面 Drawings

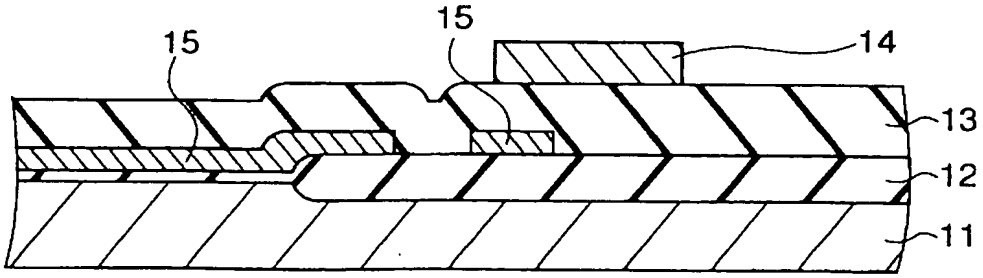
【図1】 Fig. 1



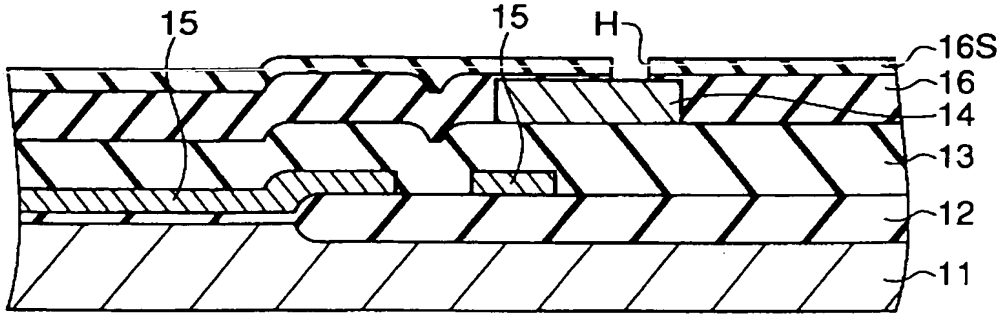
【図2】 Fig. 2



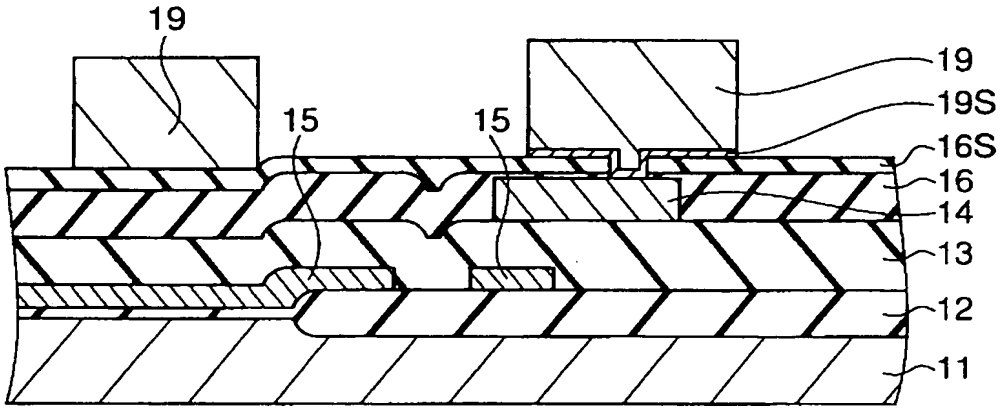
【図3】 Fig. 3



【図4】 Fig. 4



【図5】 Fig. 5



【図6】 Fig. 6